ABSTRACT

Content addressable memory (CAM) in which search results such as an address code and an array match signal can be obtained for multiple search widths. The CAM includes a CAM array that can provide match signals and suppress signals for memory locations. Match combining circuitry combines the match signals for memory locations to obtain combined match signals; the combination depends on an indicated search width, which can be one of a set of multiples of the memory location width. A priority encoder provides a priority signal indicating a combined match signal that has priority and is asserted; the priority encoder can therefore be smaller than would be necessary to prioritize all the match signals. An address encoder obtains most significant bits of an address code in response to the priority signal. Select circuitry responds to the priority signal by selecting match signals and suppress signals for the combined match signal with priority. The selected match signals are used to obtain least significant bits (LSBs) of the address code in accordance with the search width. The LSBs, selected suppress signals, and a PE match signal from the priority encoder are used to obtain an array match signal.